AMENDMENTS

In the Claims

Please amend claims 2-6, 8 and 12-13 as follows.

2. (twice amended) The method of claim [11] 16 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. (twice amended) The method of claim [11] 16 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. (twice amended) The method of claim [11] 16 wherein the second substrate is a second semiconductor substrate.

5. (twice amended) The method of claim [11] 16 wherein the first semiconductor substrate is thicker than the second substrate.

6. (twice amended) The method of claim [11] 16 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

8. (twice amended) The method of claim [11] 16 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

12. (twice amended) The method of claim [11] 16 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. (twice amended) The method of claim [11] 16 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.

Please add new claim 16 as follows.

16. (newly added) A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication;

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a removal method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, where the removal method employs the dielectric isolated metallization pattern as a stop layer.